Marked up paragraph at page 4, lines 1-10.

In Figure 1(h), a collector pedestal implant 20 for a high f_T device is formed beneath the p-type SiGe base in n^- region 5. Implant 20 is self-aligned to the emitter opening and extrinsic base implant regions and is an n-type implant. (The variable f_T is the cutoff frequency of the transistor and is an important figure of merit for high-frequency and microwave transistors. It is defined as the frequency at which the common emitter short-circuit current gain is unity. The cutoff frequency is inversely proportional to the total emitter-to-collector delay time t_{ec}. As a figure of merit, it is indicative of the raw speed at which device is capable of operating. To obtain a higher f_T, the transistor should have a very narrow base, a very narrow collector, and low capacitances.)

IN THE CLAIMS:

Please amend claims 13 as follows. A clean copy of amended claims 13 is provided in the attached separate sheet, entitled "Clean Copy of Amended Claims."

Claim 13 (Twice Amended). A heterojunction bipolar transistor, comprising:

a collector region;

a SiGe base region;

an emitter stack overlaying said [collection] collector region, said emitter stack including an emitter opening filled with T-shaped polysilicon, said T-shaped polysilicon overlaying nitride regions included in said stack; and

one and another extrinsic base regions arranged on respective sides of said emitter stack, said extrinsic base regions being directly aligned with said emitter polysilicon region but not being directly aligned with said emitter opening.

REMARKS

Minor corrections of the specification have been done by this amendment.

Claims 1-16 are currently pending in the application. Claims 1-12 have been withdrawn.

By this amendment, claim 13 is amended. Attached hereto is a separate sheet entitled "Clean Copy of Claims" showing a clean copy of the amended claim 13, and a separate sheet entitled "Clean Version of Changes to Specification" showing the clean copy of replacement paragraph to the specification. Support for the amendments in at least Figure 2G and at page 14, lines 16-20 of the present specification. No new matter is added. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Claims 13, 14 and 16 have been rejected under 35 U.S.C. §102(e) as being anticipated by Chantre et al. (U.S. Patent 6,177,717) and claims 13 and 15 have been rejected under 35 U.S.C. 102(b) as being anticipated by the admitted prior art. This rejection is respectfully traversed based on the following discussion.

The present invention focuses on creating a bipolar transistor with the improved performance characteristics. Specifically, a formation of a non-self-aligned emitter without using a traditional emitter pedestal and self-aligned extrinsic base structures help to avoid the formation of contact and mesa isolation structures which impair the performance of conventional non-self-aligned HBT devices. Compared with known self-aligned devices, total base resistance is reduced by reducing dimensions of the extrinsic base regions and allows to reduce an emitter-base junction capacitance.

The patent to Chantre et al. resolves a different problem of improving bipolar transistor parameters by eliminating an emitter/base oxide layer. As is well known, this layer limits the hole current in the base because injected electrons continue to flow due to the tunnel effect. Additionally, the dimensional characteristics of the oxide layer at the base/polysilicon-emitter interface have an influence on the static parameters of the transistor, especially it's gain. In order to resolve these problems Chantre et al. provides a way of producing an epitaxially grown single-crystal emitter directly on the base to avoid the problem of the presence of an interface oxide layer. It is very clear that structurally and technologically this reference shows different transistor which is created without concern of alignment. More particularly, referring to Figure 6 of the reference and to column 2, lines 27 *et seq.*:

> "...the invention provides a way of producing an epitaxially grown single-crystal emitter directly on the "base" (in fact, the emitter/base junction defining

the upper part of the intrinsic base lies in the upper encapsulation layer) so as to avoid the problem of the presence of an interfacial oxide layer. Consequently, the single-crystal emitter grown epitaxially, which means that there is no interfacial oxide...". (emphasis added)

The emitter, taught by Applicant, has multiple layers which formed by oxide, nitride, and TEOS layers.

Furthermore, the base in the Chantre et al. comprises the non-selective epitaxially grown stack of layers with at least one SiGe layer. (Column 2, lines 14-26) In contrast, the Applicant's base formed from single SiGe layer, implanted with p-type dopant fo form an extrinsic p+ base implant regions 70. Additionally, "These implant regions are advantageously aligned using the nitride-capped emitter stack as a mask." (Page 14, lines 16-20 of the present application) It should be noted that the alignment is not described by the reference relied on by the Examiner.

Applicant believes that the emphasizing the distinction of the present invention in the view of the admitted prior art should be addressed first in order to better convey an understanding of the invention as it distinguishes from the prior art including the reference to Chantre et al. of the present invention. More specifically, referring to the Figure 1D, representing an admitted prior art, Applicant points out that the alignment of the extrinsic base region was performed relatively to emitter opening and the sidewalls of the emitter stack were used as a masking layers for implantation of p-type dopant forming extrinsic base regions. Applicant respectfully points out to the Examiner that rejection in a view of the admitted art is not proper for the simple reason that the extrinsic base regions of the admitted prior art are self-aligned with the second polysilicon layer and the emitter pedestal, as can be appreciated from Figure 1D wherein the side walls of emitter stack are used as spacers for the intrinsic base implant. According to the present invention the emitter pedestal is made without side walls to have a width which maybe slightly wider than the emitter opening but still narrower than if formed with sidewalls and is this not aligned with than the emitter opening. The base implant can be made closer to the extrinsic base by direct alignment to polysilicon. This results in the implanted extrinsic SiGe polysilicon base regions, being self-aligned with the second polysilicon layer in the emitter pedestal, and the emitter opening. Such alignment allows create the extrinsic base regions really smaller than in

Figure 1 shown and subsequently having less total base resistance. Such reduced dimensional characteristics of the extrinsic base regions have a significant influence on the parameters of the transistor, especially its gain.

The same is true of the second embodiment of Chantre et al. (Figures 7-11) where the emitter pedestal corresponds to the emitter opening and sidewalls on the emitter pedestal provide the exitrinsic base implant mask. While the reference for alignment is less clear on the first embodiment of Chantre et al. due to the T-shaped polysilicon cross section, use of spacers remains evident and apparently necessary while prevents alignment with the polysilicon and certainly not direct alignment therewith.

Therefore it is clear that the admitted prior art as well as the reference to Chantre et al. are not concerned with sizing and the extrinsic base resistance for high performance and sidewalls appears necessary.

To emphasize the distinction of the present invention, claim 13 is amended. More specifically, claim 13 as amended now recites:

" 13. A heterojunction bipolar transistor, comprising:

...

one and another extrinsic base regions arranged on respective sides of said emitter stack, said extrinsic base regions being **directly aligned** with said emitter polysilicon region but not being directly aligned with said emitter opening; " (Claim 13 as amended, emphasis added)

Summarizing, the discussed above Applicant respectfully points out to the Examiner to the distinguishable points of the present invention which are not shown by the reference to Chantre et al.:

- multilayered emitter or emitter stack;
- single intrinsic base with two directly aligned extrinsic regions.

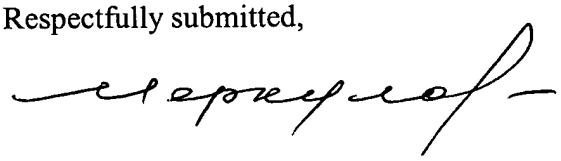
Furthermore, MPEP 2131 mandates that "**TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT IN THE CLAIM**". Additionally, the MPEP, citing *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1051, 1053 (Fed. Cir. 1987), states "[t]he identical invention must be shown in as complete detail as is contained in the ...claim" (emphasis added).

Here, none of the structural limitations highlighted in Applicant's claims above are taught or suggested by Chantre et al. or the admitted prior art. It is therefore respectfully submitted that the rejections to the claims are improper under §102 as Chantre et al. cannot anticipate the rejected claims since it does not "teach the identical invention". Further, since the above limitations are not taught or suggested, Chantre et al. cannot be used to support a *prima facie* obviousness rejection under §103. Based on the above discussion with reference to the MPEP guidelines, it is respectfully requested that the rejections based on 35 U.S.C. 102 be withdrawn.

This being the only rejection to claims 13 and 15 it is respectfully requested that these claims be allowed. For the reasons advanced, it is respectfully submitted that independent claim 13 as amended clearly define over the prior art relied on by the Examiner. The rejected claim 15 is depended on the claim 13 and allowable for this mere reason.

In view of the foregoing amendments and remarks, Applicant submits that all of the claims as amended are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicant hereby makes a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0458 (Fishkill, IBM.).

Respectfully submitted,



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